

## TSM9N90CZ C0G-VB Datasheet

### N-Channel 900V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	900
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.95
$Q_g$ (Max.) (nC)	200
$Q_{gs}$ (nC)	24
$Q_{gd}$ (nC)	110
Configuration	Single

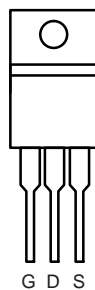
#### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

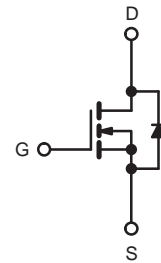


Available  
**RoHS\***  
COMPLIANT

TO-220AB



Top View



N-Channel MOSFET



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	900	V	
Gate-Source Voltage		$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	7.0	A
			$T_C = 100\text{ }^\circ\text{C}$	5.5	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	21		
Linear Derating Factor			1.5	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	770	mJ	
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	7.8	A	
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	19	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	190	W	
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	2.0	V/ns	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 23\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 7.8\text{ A}$  (see fig. 12).
- $I_{SD} \leq 7.8\text{ A}$ ,  $dI/dt \leq 140\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600\text{ V}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.65	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	900	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.98	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$	-	-	100	$\mu\text{A}$
		$V_{DS} = 720\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5.6\text{ A}^b$	-	0.95	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 100\text{ V}, I_D = 5.6\text{ A}^b$	5.6	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	3100	-	pF
Output Capacitance	$C_{oss}$		-	800	-	
Reverse Transfer Capacitance	$C_{rss}$		-	490	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 3.8\text{ A}, V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	200	nC
Gate-Source Charge	$Q_{gs}$		-	-	24	
Gate-Drain Charge	$Q_{gd}$		-	-	110	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 5.6\text{ A}, R_g = 6.2\text{ }\Omega, R_D = 52\text{ }\Omega$ see fig. 10 <sup>b</sup>	-	19	-	ns
Rise Time	$t_r$		-	38	-	
Turn-Off Delay Time	$t_{d(off)}$		-	120	-	
Fall Time	$t_f$		-	39	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	5.0	-	nH
Internal Source Inductance	$L_S$		-	13	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.0	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	21	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 5.6\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 5.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	650	980	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.8	5.7	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

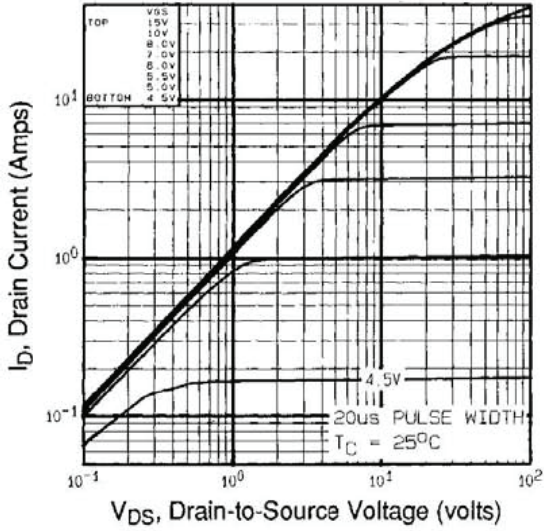


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

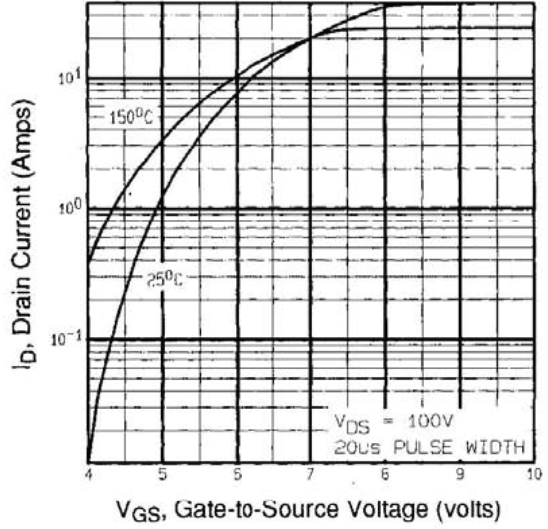


Fig. 3 - Typical Transfer Characteristics



Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

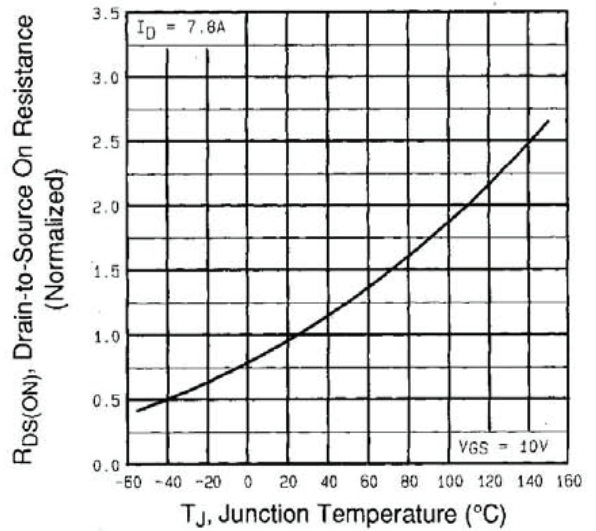


Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

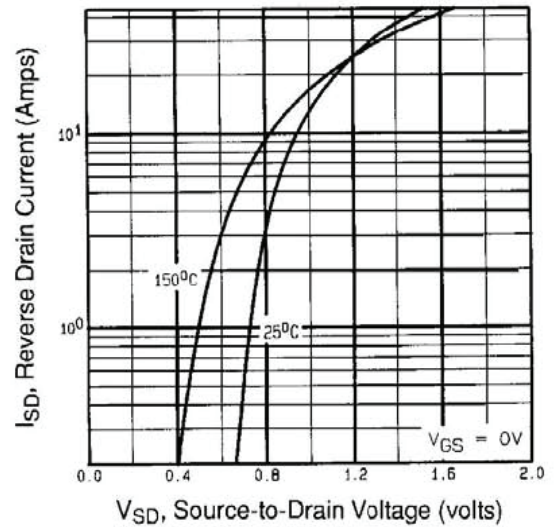


Fig. 7 - Typical Source-Drain Diode Forward Voltage

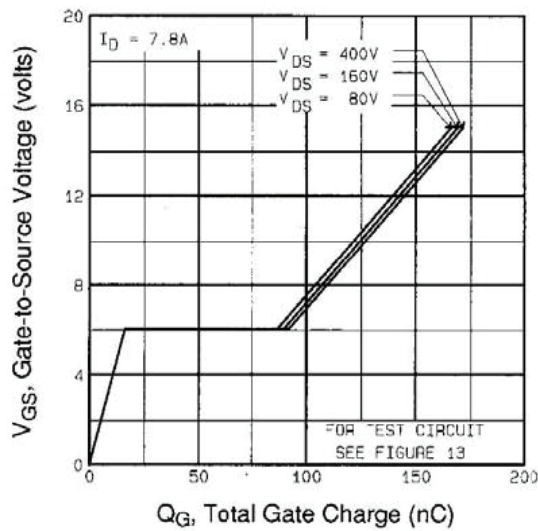


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

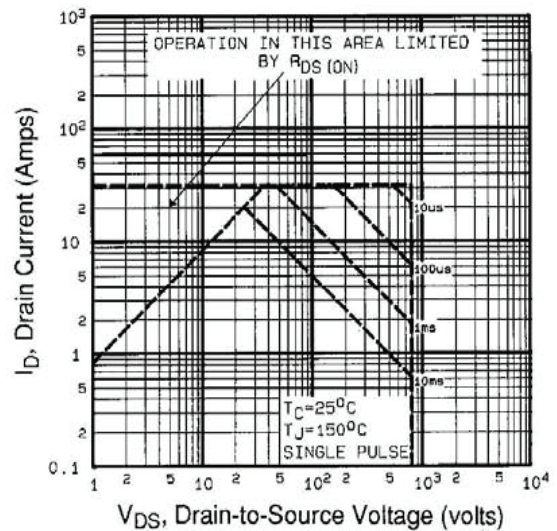


Fig. 8 - Maximum Safe Operating Area

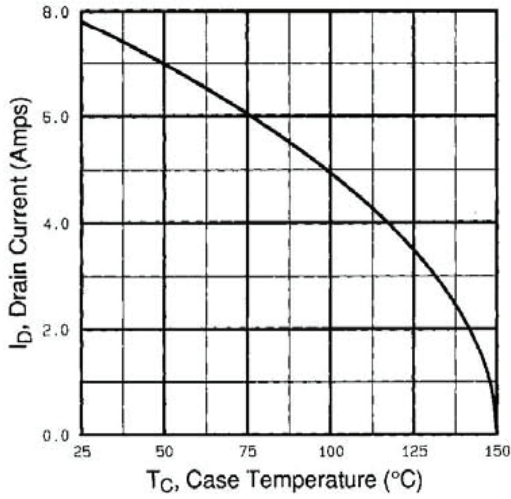


Fig. 9 - Maximum Drain Current vs. Case Temperature

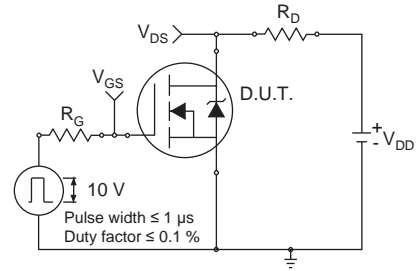


Fig. 10a - Switching Time Test Circuit

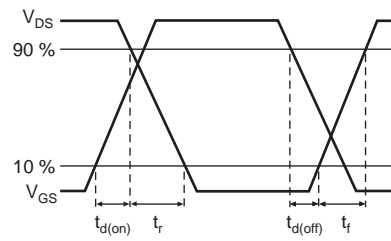


Fig. 10b - Switching Time Waveforms

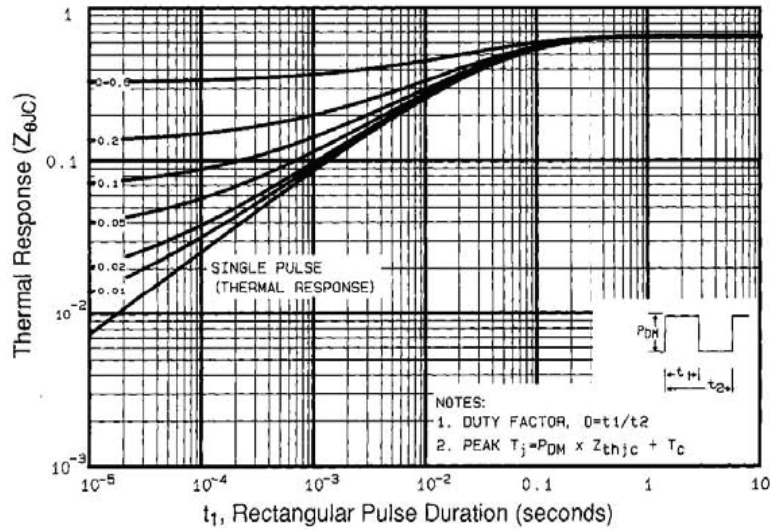


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

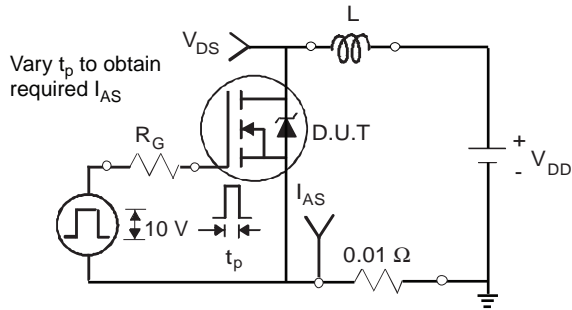


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

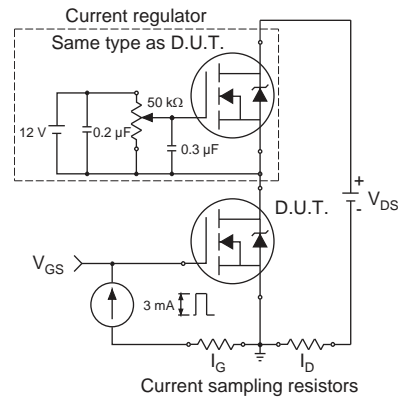
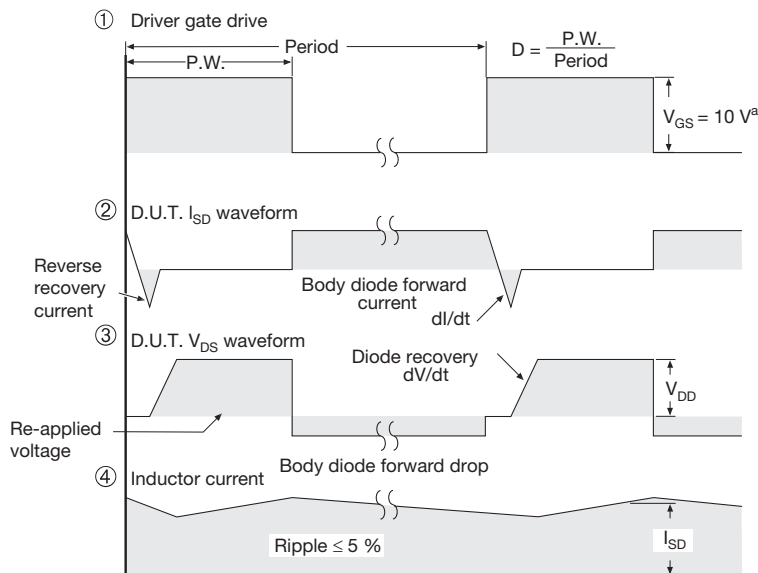
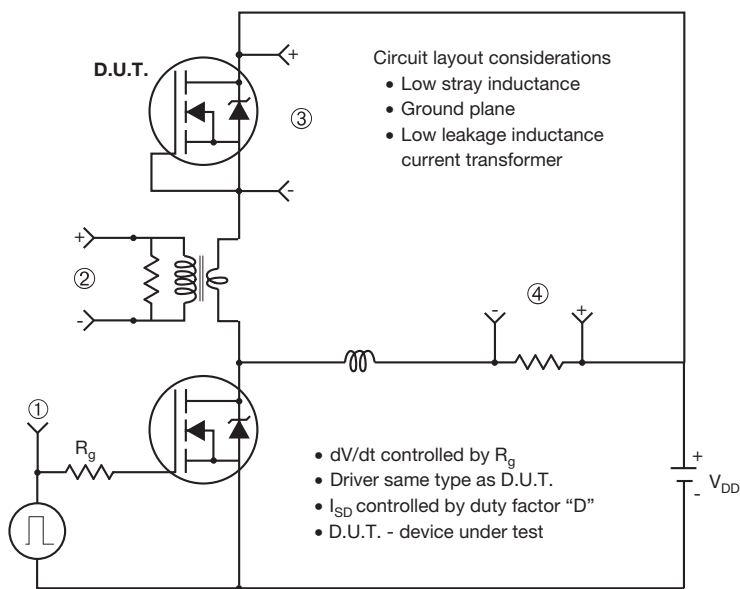


Fig. 13b - Gate Charge Test Circuit

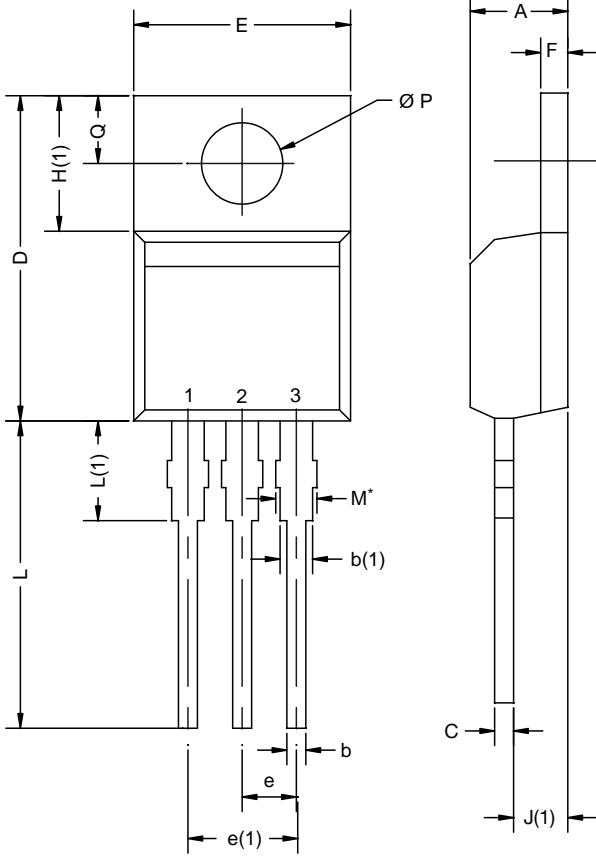
**Peak Diode Recovery dV/dt Test Circuit**



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12  
DWG: 5471

Notes

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



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